REMARKS

In the Office Action dated November 21, 2006, the Examiner has indicated the allowable subject matter of claims 3, 5, 6, 8, 10, 11, 14, 16, 17, 19-22, 25, 27 and 28, and states that the claims are allowable if rewritten in independent form with all limitations of base claims and any intervening claims. Claims 7 and 18 were rejected in the Office Action under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,649,090 to Edwards, et al. ("Edwards"). Claims 1-2, 12-13 and 23-24 were rejected under 35 USC § 103(a) by US Patent No. 6,061,750, to Beardsley (Beardsley I) in view of Edwards. Claims 4, 15 and 26 were rejected under 35 USC § 103(a) by Beardsley I combined with Edwards, and further in view of US Patent No. 5,513,097 to Beardsley (Beardsley II). Claim 9 was rejected under 35 USC § 103(a) by Edwards in view of Beardsley II.

Applicants thank the Examiner for the indication of allowability of claims 3, 5, 6, 8, 10, 11, 14, 16, 17, 19-22, 25, 27 and 28. Applicants, however, believe strongly in the patentability of the base claims from which the objected-to claims depend, particularly in view of Edwards under § 102, and in view of Beardsley I and Edwards, Beardsley I combined with Edwards, and further combined with Beardsley II, and in view of Edwards and Beardsley II under § 103. Hence, applicants have opted not to amend the objected-to claims in view of their stated allowability, but to provide the below arguments for the patentability of both the objected to claims, and the independent claims from which they depend.

Response to Rejection under § 102

In response to the rejection of claims 7 and 18 under Section 102(b) in view of Edwards, applicants respectfully assert that claims 7 and 18 patentably distinguish over Edwards, and are therefore allowable, for at least the reasons set forth below. The Examiner is thus asked to reconsider and to withdraw the rejection of claims 7 and 18 in view of Edwards, and to allow the claims.

Broadly, applicants' invention relates to a storage controller, and a method of operating a storage controller. Applicants' storage controller is for interfacing between a plurality of host systems and a direct access storage devices system. The storage controller includes a first cluster including a first processor and a first cache, and a second cluster including a second processor

and a second cache. The method includes directing data from the host systems through first and second data paths in the storage controller to the direct access storage system. Accordingly, the first processor and the first cache are associated with the first data path, and the second processor and the second cache are associated with the second data path.

Under a first set of defined conditions, the controller enters into a failover mode, wherein data directed to the first data path are routed to the second data path. Under a second set of defined conditions, the controller deconfigures the first cache without entering the failover mode. The first cache includes a series of memory pages. Preferably, the deconfiguring step includes the steps of identifying selected pages of the first cache, marking each of said selected pages as unavailable, and after all of said selected pages are marked as unavailable, removing the selected pages from the first cache.

In particular, applicants' independent claim 7 sets forth a method of deconfiguring a memory cache including a series of memory pages. The method includes identifying selected pages of the cache, marking each of said selected pages as unavailable, and after all of said selected pages are marked as unavailable, removing the selected pages from the cache.

Applicants' independent claim 18 sets forth a system for deconfiguring a memory cache that includes a series of memory pages. The controller includes means for identifying selected pages of the cache, means for marking each of said selected pages as unavailable and means for removing the selected pages from the cache after all of said selected pages are marked as unavailable.

Edwards, as distinguished from claims 7 and 18, discloses a fault tolerant computer system including at least two central processing units with cache memories and a parity error detector adapted to sense parity errors in blocks of information read from and written to cache. The Edwards' invention then issues a cache parity read or write error flag if a parity error is sensed. A system bus couples the CPU to a system control unit with a parity error corrector, and a memory bus couples the SCU to a main memory. Edwards further includes an error recovery control feature across the CPUs, a service processor and the operating system software. The error recovery control feature is responsive to the sensing of a read parity error flag in a sending CPU and a write parity error flag in a receiving CPU in conjunction with a siphon operation.

The siphon operation is intended for transferring the faulting block from the sending CPU to the main memory via the SCU (in which the given faulting block is corrected), and for subsequently transferring the corrected memory block from main memory to the receiving CPU when a "retry" is initiated.

Edwards is not found to disclose a system or method for deconfiguring a memory cache including a series of memory pages by identifying selected pages of the cache, marking each of said selected pages as unavailable, and after all of said selected pages are marked as unavailable, removing the selected pages from the cache.

While the Examiner states that Edwards, at col. 8, lines 65-66, discloses "identifying selected pages of the first cache," applicants, with all due respect, disagree. Applicant reads the cited Edwards' text as "B) Provide information relating to the error (including the identity of the associated cache block)." This is not the equivalent of "identifying selected pages of the cache;" applicants' claimed element. That is, in step "A", Edwards detects an error, and then provides information relating to the error including the identity of an associated cache block. Nowhere does Edwards mention "selected pages of the first cache," which presumes that errors in the first cache are already identified. Applicants believe that "identifying selected pages of the cache;" obviates any need for carrying out the Edwards task of identifying an associated cache block containing an error.

While the Examiner cites Edwards' col. 7, lines 41-43 as disclosing the claimed step of "marking each of said selected pages as unavailable," applicants do not agree. Nowhere in the cited text does Edwards refer to selected pages, or marking selected pages. Edwards refers only to invalidating a block of data held by the receiving CPU based on fetched row and level information identifying the block from both the sending and receiving CPUs. And the Edwards' text cited at col. 7, lines 52-55, and col. 9, lines 4-5, does not disclose or describe a step of "after all of said selected pages are marked as unavailable, removing the selected pages from the first cache." Edwards' cited text merely describes that the SP disables storage elements in the cache associated with the failing block by disabling its level after the swap completes. Edwards does not appear to be concerned about individual pages of a cache at all.

Applicants conclude and respectfully assert, therefore, that their independent claims 7 and 18 are not anticipated under Section 102(b) by Edwards, and request withdrawal of the 102(b) rejection of claims 7 and 18.

Response to Rejection under § 103

With respect to the rejection of claims 1-2, 12-13 and 23-24 under 35 USC § 103(a) by Beardsley I in view of Edwards, the Examiner states that Beardsley I teaches operating a storage controller for interfacing between a plurality of host systems (Fig. 3-34, 36) and a direct access storage device system (Fig. 3-4, 6), including a first cluster with a first processor and a first cache (Fig. 3-12, 16), and a second cluster with a second processor and cache (Fig. 3-14, 18). The Examiner further states that applicants' step of directing data is found at Beardsley I col. 2, line 66, through col. 3, line 15, and the step of entering at col. 3, lines 15-22.

The Examiner asserts further that Beardsley I does not teach a second set of defined conditions, deconfiguring the cache without first entering the failover mode, except for overcoming storage controller failures, but that Edwards teaches deconfiguring a first cache without entering failover mode (col. 1, lines 51-52). The Examiner concludes that it would have been obvious to combine the first cache configuration of Edwards with the fault handling structure of Beardsley I to realize applicants invention as set forth by the language of independent claims 1, 12 and 23. The Examiner concludes that the motivation for the combination is found in Edwards by their desire to find a way to continue processor operation in view of error (col. 2, lines 52-54).

Applicants respectfully disagree that the Examiner has met his burden of establishing motivation under Section 103(a), required by law to maintain the obviousness rejection. That is, applicants believe that there are many techniques and corresponding structure known in the art for "continuing processor operation in view of error," but that the Examiner's statement is insufficient motivation under the law for maintaining the rejection. The US Federal Circuit has made clear that virtually all inventions are combinations of old elements, and that an Examiner may often find every element of a claimed invention in the prior art. Hence, to prevent the use of hindsight to defeat patentability, US patent examiners are required to show some motivation to

combine the references to maintain the obviousness rejection. In re Rouffet, 47 USPQ2d 1457-58 (Fed. Cir. 1998).

Beardsley I teaches a failover system for a DASD storage controller. At Beardsley I's col. 3, lines 15-22, it is stated that upon determining that the second processor has failed, the first processor configures the second host adaptor and second device adaptor to communicate with the first processor. Thereafter, I/O requests from a host system to the second DASD are transferred via the second host adaptor, the first processor and second host adaptor. The Beardsley I path referred to is through the second host adaptor, the first processor and the second host adaptor. Applicants' first path includes only a first processor and first cache. Edwards is a fault tolerant computer system. There is no motivation found in either reference for combining a fault tolerant computer system of Edwards into a DASD storage controller. It just does not make sense, and the combination is believed to be unworkable.

But even *assuming arguendo* that there is some reason, motivation or suggestion for combining the Edwards into Beardsley I, such combination still would not render obvious applicants' invention as set forth in the rejected claims. For example, Edwards does not teach deconfiguring a first cache without entering a failover mode at col. 1, lines 51-52, but instead that "2. A sophisticated machine should support the deconfiguration of a failing cache storage element." Applicants' invention is not constructed as is Edwards, for merely deconfiguring a cache, but for deconfiguring pages in a cache.

The Examiner further supports the § 103(a) rejections by asserting that applicants' step: under a first set of defined conditions, entering into a failover mode, wherein data directed to the first data path are routed to the second data path, is found in Beardsley I at col. 3, lines 15-22. Applicants' reading of the cited Beardsley I text does not find mention of routing data at all. Beardsley I at col. 3, lines 15-22, merely states that "upon determining that the second processor has failed, the first host processor configures the second host adaptor... After configuration in response to determining that the second processor has failed, an I/O request ... is transferred via the second host adaptor, the first processor, and the second device adaptor." Consequently, and as already stated, combining Edwards into Beardsley I does not realize an invention as set forth in applicants' independent claims.

Applicants, therefore, respectfully assert that independent claims 1, 12 and 23 are not obvious under 103(a) by combining Edwards into Beardsley I, and the claims are patentable. Moreover, because claims 2, 13 and 24 depend from claims 1, 12 and 23, respectively, applicants assert that those claims are also patentable under 103(a) in view of the proposed combination for at least the reasons set forth for the patentability of the independent claims. Accordingly, applicants request withdrawal of the rejection of claims 1, 2, 12, 13, 23, 24 under § 103(a) by Beardsley I in view of Edwards.

With respect to the rejection of claims 4, 15 and 26 under 35 USC § 103(a) by Beardsley I combined with Edwards, and further in view of Beardsley II, applicants respectfully assert that claims 4, 15 and 26, which depend from independent claims 1, 12 and 23, respectively, are patentable under Section 103(a) by Beardsley I combined with Edwards, and as further combined with Beardsley II, for at least the reasons set forth above for the patentability of independent claims 1, 12 and 23 in view of the Beardsley I/Edwards proposed combination. Applicants therefore respectfully assert that claim 1, 12 and 23 are non-obvious under Section 103(a) in view of Beardsley I and Edwards, the combination combined with Beardsley II, and request withdrawal of the rejection of claims 4, 15 and 26 under 35 USC § 103(a), by the proposed combination.

With respect to the rejection of claim 9 under 35 USC § 103(a) by Edwards in view of Beardsley II, the Examiner asserts that Edwards teaches applicants invention as set out in claim 9 except for: "that for each of the selected pages, determining whether the page is modified or unmodified," and where it was modified, "processing the page according to a defined routine, and then marking the page as unavailable." The Examiner then suggests that Edwards teaches removing cache portions, that Beardsley II teaches determining whether a page is modified or unmodified, and where modified, processing by a defined routine and marking the page as unavailable. The Examiner asserts in conclusion that it would have been obvious to combine the scan and destage operations of Beardsley II with the Edward's cache disabling to realize applicants claim 9 invention. The Examiner then further asserts that that the motivation is present because "identifying and processing modified data helps to ensure data integrity" (Beardsley II, col. 2, lines 31-40).

Applicants respectfully disagree for at least the following reasons. Claim 9 depends from claim 7. Applicants clearly distinguished Edwards from claim 7 in response to the Examiner's argument rejecting claims 7 and 18 under Section 102(b) in view of Edwards. While the Examiner asserts broadly that the motivation for such a combination is inherent because "identifying and processing modified data helps ensure data integrity," applicants disagree. There is no motivation found in either reference for combining Edwards' fault tolerant multiprocessor with Beardsley II's method and system for maintaining information about modified data in a cache in a storage system for use in a system failure.

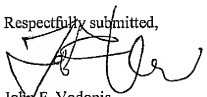
But even assuming arguendo that there could be a motivation to combine, such a hypothetical combination would still not realize an invention as set forth in claims 9/7. That is, Edwards does not teach deconfiguring a first cache without entering a failover mode at col. 1, lines 51-52, but instead that "2. A sophisticated machine should support the deconfiguration of a failing cache storage element." And while Beardsley II information maintenance system includes a system for caching data, nowhere does Beardsley II's disclose, teach or suggest processing a modified page according to a defined routine and marking the page as unavailable. Hence combining Edwards and Beardsley II would not realize applicants' invention as set forth by the claim 9 language. Applicants respectfully assert, therefore, that claim 9 is not obvious under Section 103(a) by Beardsley II combined into Edwards, and respectfully request withdrawal of the claim 9 rejection.

In view of the above-discussed differences between presently pending claims 1, 2, 4, 7, 9, 12, 13, 15, 18, 23, 24 and 26, and Edwards, Beardsley I in view of Edwards, Beardsley I and Edwards combined with Beardsley II, and Edwards combined with Beardsley II, and because of the advantages associated with those differences, claims 1, 2, 4, 7, 9, 12, 13, 15, 18, 23, 24 and 26 patentably distinguish over the cited art and are allowable under Section 103(a). For that matter, claims 3, 5, 6, 8, 10, 11, 14, 16, 17, 19-22, 25, 27 and 28, which were objected to, are believed allowable in view of the arguments for patentability set forth above for independent claims 1, 7, 12, 18 and 23, from which they respectively depend. Accordingly, applicants request withdrawal of the objections to those claims.

The other references have been reviewed, and these other references, whether considered individually or in combination, also do not disclose or anticipate this feature of the present invention. Hence, in light of the above-discussion, the Examiner is respectfully requested to reconsider and to withdraw the rejection of claims 1-28 and allow those claims.

If the Examiner believes that a telephone conference with Applicant's Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned at 516 742 4343.

Respectfully submitted,



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